The Third NASA/DoD Workshop on Evolvable Hardware

July 12-14, 2001
Rennaissance Long Beach Hotel, Long Beach, California, USA
Jet Propulsion Laboratory, California Institute of Technology

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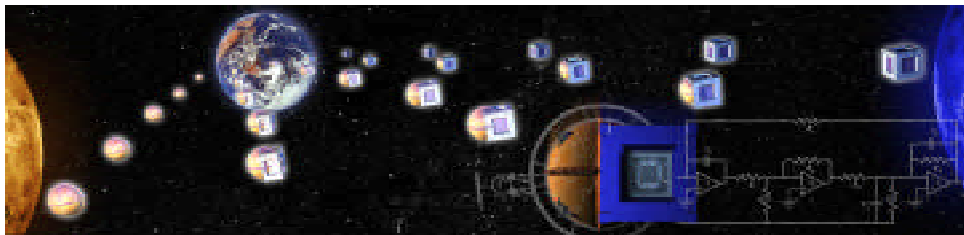
The Third NASA/DoD Workshop on Evolvable Hardware (EH-2001) will be held at the Rennaissance Long Beach Hotel, Long Beach, California and hosted by the Jet Propulsion Laboratory, California Institute of Technology. Evolvable Hardware is an emerging field that applies evolution to automate design and adaptation of physical structures such as electronic systems, antennas, MEMS and robots. The purpose of this workshop is to bring together leading researchers from the evolvable hardware community, representatives of the automated design and programmable/reconfigurable hardware communities, technology developers, and end-users from the aerospace, military and commercial sectors.

Evolvable hardware techniques enable self-reconfigurability and adaptability of programmable devices and thus have the potential to significantly increase the functionality of deployed hardware systems. Evolvable Hardware is expected to have major impact on deployable systems for space missions and defense applications that need to survive and perform at optimal functionality during long duration in unknown, harsh and/or changing environments. Evolvable hardware is also expected to greatly enrich the area of commercial applications in which adaptive information processing is needed; such applications range from human-oriented hardware interfaces and internet adaptive hardware to automotive applications.

The focus of this year's workshop will be to provide a roadmap from the current proof-of-concept stage of Evolvable Hardware to the development of larger scale real world systems addressing issues such as evolvability and scalability. The Workshop attendees will have the opportunity to discuss the fundamental issues and state-of-the art of evolvable hardware technology, plans for development of future devices and hardware systems suitable for evolution, and needs related to space applications.

Registration & check-in information

The meeting will begin at 9:00 A.M. on Thursday, July, 12, at the Renaissance Long Beach Hotel in the BallRoom. This room is located on the second floor of the Renaissance Long Beach Hotel building, adjacent to the lobby. There is covered parking at $5.00/day; access is off of Pine Avenue north of the Renaissance Long Beach Hotel building. On-site check-in will begin on Wednesday, July 11 from 6:00 P.M. to 8:00 P.M and Thursday, July 12 at 8:00 A.M. at the meeting site. At this time, you will be given your meeting badge and receipt for the registration fee, plus a packet of meeting materials. Two social events are being planned as part of the workshop. On Thursday, July 12, there will be a reception. On Friday, July 13, there will be a group dinner. It is hoped your schedule will allow for your participation in both of these opportunities for continued discussion following each day's presentations. All participants will be expected to pay the workshop registration fee of $300.00 which covers the cost of the workshop, plus break service, a lunch Thursday July 12, a reception and a group dinner. Please make checks payable to Caltech and forward per instructions on the registration form. Note that no purchase orders, foreign checks or foreign currency can be accepted. Credit Cards (VISA, MASTER and AMERICAN EXPRESS) and US dollar traveler's checks are accepted. For our planning purposes, pre-registration with payment of fees on our workshop web site is appreciated.

Accommodation and transportation

A block of rooms has been set aside at the Renaissance Long Beach Hotel at the current goverment rate of $99/single or double occupancy plus tax and at the non-government rate of $129/single or double occupancy plus tax. The hotel will hold the room block until June 20, 2001 or until it is filled, after which time they will honor the rate on a space available basis only. You are responsible for making you own arrangements directly with the hotel. The Long Beach area is served by three major airports: Los Angeles International airport (LAX), John Wayne(SNA) and Long Beach(LGB). There are several shuttles which provide door-to-door, on-call van service from the airports to Renaissance Long Beach Hotel. At LAX, to board the shuttles, exit the baggage claim area outside the terminal, look at the van stop sign located on the central island and contact the guest service shuttle representative. Purchase tickets from the driver (around $15 to $20 from LAX to Renaissance Hotel). Taxis and rental cars are also readily available at the airports and in Long Beach. For further information, call:

Renaissance Long Beach Hotel
111 East Ocean Boulevard, Long Beach, CA 90802
Phone: +1 (562) 437-5900   Fax: +1 (562) 499-2509
Reference: Evolvable Hardware

Super Shuttle: (800) 258-3826
Prime Time: (800) 733-8267

For further information please check the workshop web site or contact

Web Site: http://cism.jpl.nasa.gov/ehw/events/nasaeh01

Technical: Didier Keymeulen
Jet Propulsion Laboratory, MS 303-300
4800 Oak Grove Drive, Pasadena, CA 91109, USA
didier.keymeulen@jpl.nasa.gov
Tel: +1 (818) 354-4280   Fax: +1 (818) 393-1545

Conference Logistics: Pat McLane
Patricia.B.Mclane@jpl.nasa.gov
Tel: +1 (818) 354-5556   Fax: +1 (818) 393-4992

8:00 - 9:00	**Registration**
9:00 - 9:10	**Didier Keymeulen,** Jet Propulsion Laboratory, USA **Adrian Stoica,** Jet Propulsion Laboratory, USA *Welcome and Organizational Remarks*
9:10 - 9:15	**Benny Toomarian,** Jet Propulsion Laboratory, USA *Opening Address*
9:15 - 9:25	**Henry McDonald,** NASA Ames Research, USA *Welcome Address*
9:25 - 10:00	**Richard Terrile,** Jet Propulsion Laboratory, USA *Rise of the Machines: Evolvable Hardware and Space Exploration*
10:00 - 10:45	**Stephen Trimberger,** Xilinx, USA *Reconfigurable Devices in the 21st Century*
10:45 - 11:00	*Break*
11:00 - 11:40	**Xin Yao,** University of Birmingham, UK *What Evolvable Hardware Still Can't Do?*
11:40 - 12:20	**Tetsuya Higuchi,** Electrotechnical Laboratory, Japan *Evolvable Hardware for Industrial Applications*
12:20 - 1:30	***Lunch***

Session 1: From Biology to Robotics

1:30 - 2:10	**John Koza,** Stanford University, USA *Evolving Molecular Circuits by Means of Natural Evolution*
2:10 - 2:50	**Meyya Meyyappan,** NASA AMES, USA *Nanotechnology in Information Processing: Opportunities and Challenges*
2:50 - 3:10	**Chris Leger,** Jet Propulsion Laboratory, USA *Evolutionary Design for Robot Configuration Design*
3:10 - 3:30	**Brad Dolin, F.H. Bennett III, E.G. Rieffel,** FX Palo Alto Laboratory, USA *Methods for Evolving Robust Distributed Robot Control Software: Coevolutionary and Single Population Techniques*
3:30 - 3:45	*Break*

Session 2: Bio-Inspired Systems

3:45 - 4:05	**Jose L. Segovia-Juarez,** Wayne State University, USA; **Silvano Colombano,** NASA-Ames Research Center, USA *Mutation Buffering Capabilities of the Hypernetwork Model*
4:05 - 4:25	**Jeffrey O. Pfafmann, Klaus-Peter Zauner,** Wayne State University, USA *Scouting Context-sensitive Components*
4:25 - 4:45	**John C. Gallagher,** Wright State University, USA *A Neuromorphic Paradigm for Extrinsically Evolved Hybrid Analog/Digital Device Controllers: Initial Explorations*
4:45 - 5:00	*Break*

Session 3: Applications I

5:00 - 5:20	**Derek Linden,** Linden Innovation Research, USA *A System for Evolving Antennas In-Situ*
5:20 - 5:40	**Joseph H. Saleh, Daniel Hastings, Dava Newman,** Department of Aeronautics and Astronautics, MIT *Extracting the Essence of Flexibility in System Design*
5:40 - 6:00	**Ann Garrison Darrin, Richard Conde, Bobbie Chern,** John Hopkins University, USA; **Phil Luers,** NASA Goddard Space Flight Center, USA; **Steve Jurczyk and Carl Mills,** NASA Langley Research Center, USA *Adaptive Instrument Module: Space Instrument Controller "Brain" through Programmable Logic Devices*
7:00 - 9:00	***Reception Cocktail*** Renaissance Long Beach Hotel

Friday, July 13

8:00 - 9:00 **Registration**

9:00 - 10:00 **Rob Rutenbar,** Carnegie Mellon University, USA
Synthesis for Industrial-Scale Analog Intellectual Property

Session 4: Evolution of Analog and Mixed-Signal Circuits

10:00 - 10:20 **Trent McConaghy,** Analog Design Automation, USA
A Multi-Objective hierarchical Methodology for Snthesis of Large Scale Electronic Designs

10:20 - 10:40 **Hajime Shibata, Nobuo Fujii,** Tokyo Institute of Technology, Japan
Analog Circuit Synthesis Based on Reuse of Topological Features of Prototype Circuits

10:40 - 11:00 **Adrian Stoica, Ricardo Zebulum, and Didier Keymeulen,** Jet Propulsion Laboratory, USA
Progress and Challenges in Building Evolvable Devices

11:00 -11:20 **Cristina Santini,** Catholic University of Rio, Brazil; **Ricardo Zebulum,** JPL; **Marco Pacheco, Marley Vellasco, Moises Szwarcman,** Catholic University of Rio, Brazil
PAMA-Programmable Analog Multiplexer Array

11:20 - 11:35 *Break*

Session 5: Reconfigurable Architectures and Devices

11:35- 11:55 **Juan Manuel Moreno,** Technical University of Catalunya, Spain; **Eduardo Sanchez,** Swiss Federal Institute of Technology Lausanne, Switzerland; **J. Cabestany,** Technical University of Catalunya, Spain
An In-System Routing Strategy for Evolvable Hardware Programmable Platforms

11:55 - 12:15 **R. Timothy Edwards,** John Hopkins University Applied Physics Lab, USA; **C.-J. Kim,** UCLA
Breaking the Resistivity Barrier

12:15- 12:35 **Joerg Langeheine, Joachim Becker, Simon Folling, Karlheinz Meier, Johannes Schemmel,** Heidelberg University, Germany
A CMOS FPTA Chip for Intrinsic Hardware Evolution of Analog Electronic Circuits

12:35 - 12:55 **Ed Ramsden,** Lattice Corporation, USA
The ispPAC Family of Reconfigurable Analog Circuits

12:55 - 2:00 *Lunch*

Session 6: Survivable and Flexible Hardware

2:00 - 2:40 **Miron Abramovici,** Agere Systems, USA; **John Emmert, Charles Stroud,** University of North Carolina at Charlotte, USA
Roving STARs: An Integrated Approach to On-line Testing, Diagnosis, and Fault Tolerance for FPGAs in Adaptive Computing Systems

2:40 - 3:00 **Adrian Stoica, Didier Keymeulen, and Ricardo Zebulum,** Jet Propulsion Laboratory, USA
Evolvable Hardware Solutions for Extreme Temperature Electronics

3:00 - 3:20 **A.M. Tyrrel, G. Hollingworth, S.L. Smith,** University of York, UK
Evolutionary Strategies and Intrinsic Fault-Tolerance

3:20 - 3:40 **Helio Sinohara, Marco Pacheco, Marley Vellasco,** Catholic University of Rio, Brazil
Repair of Analog Circuits: Extrinsic and Intrinsic Evolutionary Techniques

3:40 - 3:55 *Break*

Session 7: Evolution of Signal Processing Circuits

3:55 - 4:15 **Ben I. Hounsell and Tughrul Arslan,** The University of Edimburgh, UK
Evolutionary Design and Adaptation of Digital Filters Within an Embedded Fault Tolerant Hardware Platform

4:15 - 4:35 **Thorsten Schnier and Xin Yao,** The University of Birmingham, UK; **Pin Liu,** Marconi Communications
Digital Filter Design Using Multile Pareto Fronts

4:35 - 4:55 **Oscar Castillo, O. Montiel, R. Sepulveda, and P. Melin,** Tijuana Institute of Technology, Mexico
Application of a Breeder Genetic Algorithm for System Identification in an Adaptive Finite Impulse Response Filter

4:55 - 5:10 *Break*

Session 8: Evolution of Digital Functions

5:10 - 5:30 **Pauline C. Haddow and G. Tufte,** The Norwegian University of Science and Technology, Norway
Bridging the Genotype-Phenotype Mapping for Digital FPGAs

5:30 - 5:50 **Julian Miller,** University of Birmingham, UK; **Morten Hartmann,** The Norwegian University of Science and Technology, Norway
Evolving Messy Gates for Fault-tolerance: Some Preliminary Findings

7:00 - 10:00 **Banquet Dinner**
Queen Mary

Session 9: Applications II

9:00 - 9:20   **Reid Porter, Maya Gokhale, Neal Harvey, Simon Perkins, Cody Young,**   Los Alamos National Laboratory, USA
Evolving Network Architectures with Custom Computers for Multi-Spectral Feature Identification

9:20 - 9:40   **John W. Lockwood,** Washington University, USA
Evolvable Internet Hardware Platforms

9:40 - 10:00   **Robert I. Graham and Tughrul Arsian,**   University of Edimburgh, UK
Rule Evolution in Order Based Diagnosic Systems

10:00 - 10:10   *Break*

Session 10: Evolution of CA and Brain-Inspired Architectures

10:10 - 10:30   **Andre Stauffer, Daniel Mange, Gianluca Tempesti, Christof Teuscher,**   EPFL, Switzerland
BioWatch: A Giant Electronic Bio-inspired Watch

10:30 - 10:50   **Daryl Bradley, A.M. Tyrrell,**   University of York, UK
The Architecture for a Hardware Immune System

10:50 -11:10   **Alexander H. Jackson, A.M. Tyrrell,**   University of York, UK
Asynchronous Embryonics

11:10 -11:30   **Hugo de Garis, L. de Penning,**   STARLAB, Belgium; **A. Buller,** ATR, Japan; **D. Decesare**, Utah State University, USA
Early Experiments on the CAM-Brain Machine (CBM)

11:30 - 11:40   *Break*

Session 11: Evolvability

11:40 - 12:00   **S. Kazadi, Y. Qi, I. Park, H. Huang, P. Hwu, B. Kwan, W Lue, H. Li,**   Jisan Research Institute, USA
Insufficiency of Piecewise Evolution

12:00 - 12:20   **Pauline C. Haddow,**   The Norwegian University of Science and Technology, Norway and **Piet van Remortel,**
Vrije Universiteit Brussel, Belgium
From Here to There: Future Robust EHW Technologies for Large Digital Designs

12:20 - 12:40   **Arturo Hernandez-Aguirre, Bill Buckles,**   Tulane University USA, **Carlos Coello,** Cinvestav-Ipn, Mexico
On Learning kDNF Boolean Formulas

12:40 - 12:50   ***Conclusions***